High Efficiency POL Module

HM Series **HM10107A**

FEATURES:

- High Power Density Power Module
- 10A Maximum Load
- Input Voltage Range from 1.0V to 15.0V
- PVCC Voltage Range from 4.5V to 14.4V
- Output Voltage Range from 0.6V to 5.0V
- Excellent Thermal Performance
- 95% Peak Efficiency
- Enable Function
- Protections (OCP, Non-latching)
- Internal Soft Start with Pre-bias Output Start-Up
- QFN- Package 15mm*15mm*3.5mm
- Low Profile and Compact Size
- Pb-free Available (RoHS compliant)
- MSL 3, 245C Reflow

APPLICATIONS:

- General Buck DC/DC Conversion
- Distributed Power Supply
- Datacom, and Telecom Power Supplies
- Server/Desktop Power Supplies

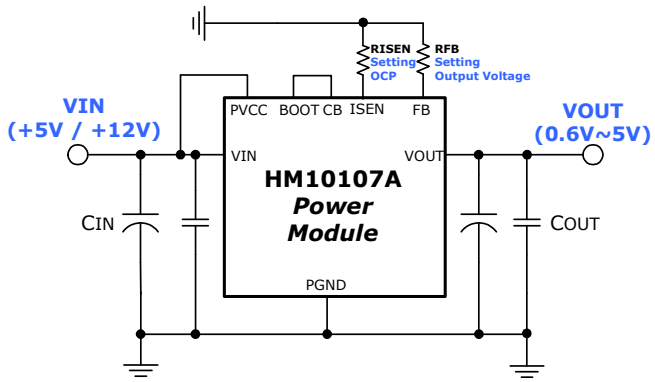
GENERAL DESCRIPTION:

The HM10107A is a high frequency, high power density and complete DC/DC power module. The PWM controller, power MOSFETs and most of support components are integrated in one hybrid package.

The features of HM10107A include voltage mode control with high phase margin compensation, internal soft-start, OCP and pre-biased output start-up capability. Besides, HM10107A is an easy to use POL module, only input capacitors and output capacitors need to design for all kinds of applications.

The low profile package enables utilization of unused space on the bottom of PC boards for highly density point of load regulation. The HM10107A is packaged in a thermally enhanced, compact (15mm×15mm x 3.5mm) and low profile QFN package suitable for automated assembly by standard surface mount equipments. The HM10107A is Pb-free and RoHS compliance.

TYPICAL APPLICATION CIRCUIT & PACKAGE SIZE:



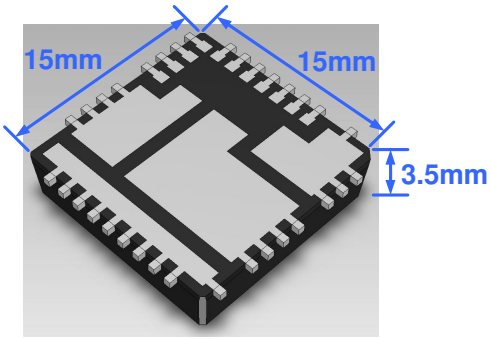


TABLE 1: OUPUT VOLTAGE SETTING

Vout	1.05V	1.2V	1.5V	1.8V	2.5V	3.3V	5V
RFB (Ohm)	13k	9.76k	6.49k	4.87k	3.09k	2.16k	1.33k

ORDER INFORMATION:

Part Number	Ambient Temp. Range (°C)	Package (Pb-Free)	MSL	Shipment
HM10107A	-40 ~ +85	QFN 15Ld.	Level 3	-

SIMPLIFIED INTERNAL BLOCK DIAGRAM:

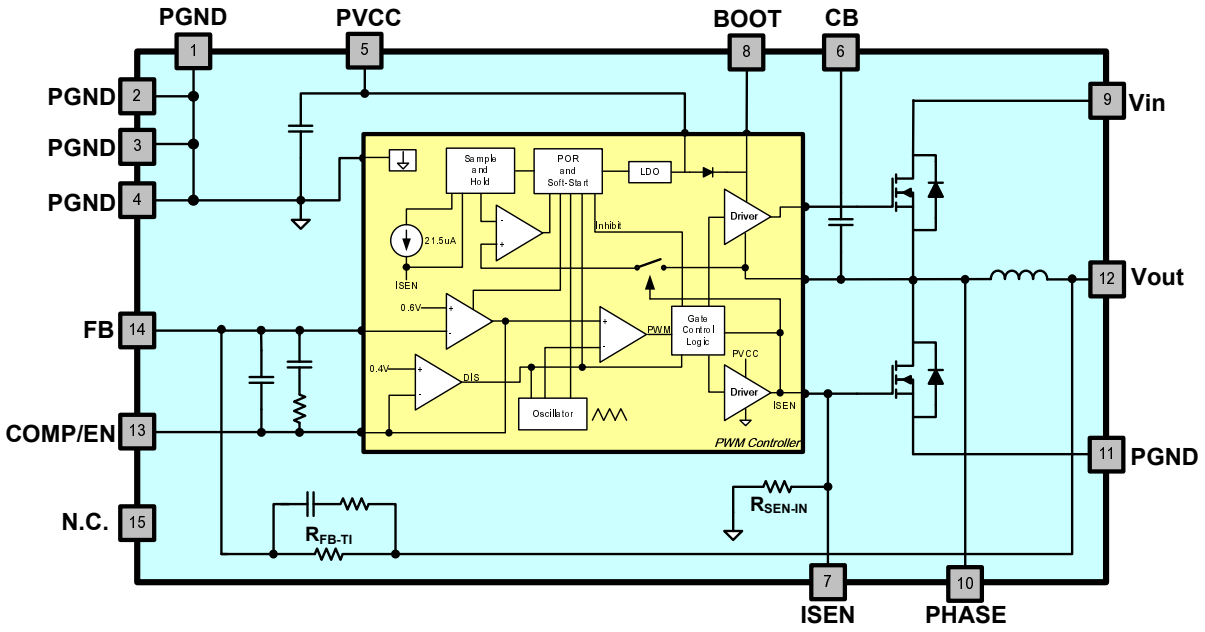
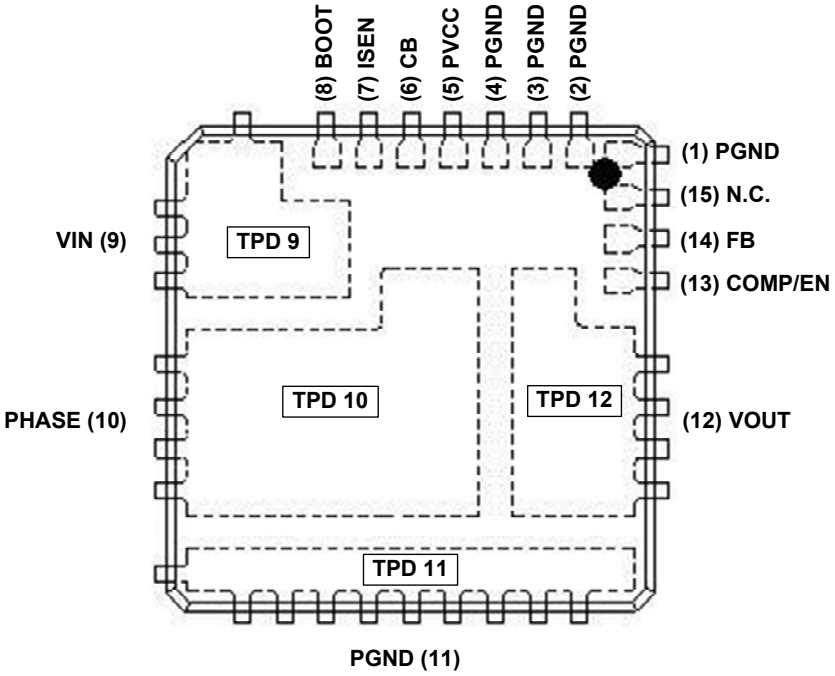


FIG.1 INTERNAL BLOCK DIAGRAM

PIN CONFIGURATION:



Top View

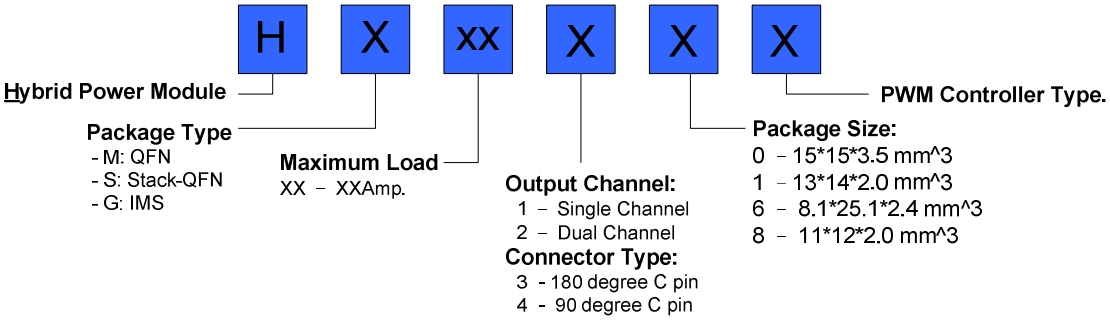
PIN DESCRIPTION:

Symbol	Pin No.	Description
PGND	1, 2, 3, 4	Power ground pin for signal, input, and output return path. This pin needs to connect one or more ground plane directly.
PVCC	5	Supply voltage pin for internal bias supply and MOSFETs gate drivers. It needs to connect 2.2uF ceramic capacitor to ground plane directly and place this capacitor as closely as possible to this pin.
CB	6	Node of internal bootstrap capacitor. Connect to BOOT pin directly for typical application.
ISEN	7	The ISEN pin is over current protection setting. It compares the $R_{DS(ON)}$ of low-side MOSFET to configure the over current protection trip current. The HM10107A has initial current setting to limit the surge current impact. It has an integrated internal 12.1kΩ resistor (R_{SEN-IN}) between ISEN and PGND pin. One can also connect external resistor (R_{SEN-EX}) between this pin and PGND pin to reduce the over current trip point. The recommendation of this external resistor (R_{SEN-EX}) is 10kΩ for general application limit .Place this resistor as closely as possible to this pin.

PIN DESCRIPTION: (Cont.)

Symbol	Pin No.	Description
BOOT	8	Node of internal bootstrap diode. Connect to CB pin directly for typical application.
VIN (TPD 9)	9	Power input pin. It needs to connect input rail and using for heat transferring to heat dissipation layer by Vias connection. Place the input ceramic type capacitor as closely as possible to this pin.
PHASE (TPD 10)	10	Phase node pin. Node of high-side and low-side MOSFETs and output inductor connection. Using for heat transferring to heat dissipation layer by Vias connection. For electrically, if voltage spike stress and EMI considered, the snubber circuit can be as closely as possible connected to this pin that will absorb the spike and ringing well.
PGND (TPD 11)	11	Power ground pin and used for both PGND pin (1, 2, 3, and 4). It needs to connect one or more ground plane directly and using for heat transferring to heat dissipation layer by Vias connection. Place the input ceramic type and output capacitors as closely as possible to this pin. If voltage spike stress and EMI considered, the snubber circuit can be as closely as possible connected to this pin that will absorb the spike and ringing.
VOUT (TPD 12)	12	Power output pin. Connect to output and using for heat transferring to heat dissipation layer by Vias connection. Place the output capacitors as closely as possible to this pin.
COMP/EN	13	This is multi-function pin for HM10107A. Compensation and enable.
FB	14	Feedback input. Connect resistor between this pin and ground for adjusting output voltage. Place this resistor as closely as possible to this pin.
N.C.	15	No function. Not connected.

PART NUMBER STRUCTURE:



PRODUCT LABEL:

ELECTRICAL SPECIFICATIONS:

CAUTION: Don not operate at or near absolute maximum rating listed for extended periods of time. This stress may adversely impact product reliability and result in failures not covered by warranty.

Parameter	Description	Min.	Typ.	Max.	Unit
■ Absolute Maximum Ratings					
PVCC to PGND		PGND-0.3	-	+15	V
CB to PHASE		-	-	+15	V
ISEN to PGND		PGND-0.3	-	PVCC+0.3	V
BOOT to PGND		PGND-0.3	-	+36	V
BOOT to PVCC		-	-	+24	V
VIN to PHASE	Note 1	-1.2	-	+30	V
PHASE to PGND	Note 1	-1.2	-	+30	V
COMP/EN to PGND		PGND-0.3	-	+6	V
FB to PGND		PGND-0.3	-	+6	V
Tc		-	-	+110	°C
Tj		-40	-	+125	°C
Tstg		-40	-	+125	°C
ESD Rating	Human Body Model (HBM)	-	-	2k	V
	Machine Model (MM)	-	-	100	V
	Charge Device Model (CDM)	-	-	1k	V
■ Recommendation Operating Ratings					
VIN	Input Supply Voltage	+1	-	+15	V
VOUT	Output Voltage	+0.6	-	+5	V
PVCC	Fixed Supply Voltage for 5V	+4.5	+5	+5.5	V
	Fixed Supply Voltage for 12V	+9.6	+12	+14.4	V
	Wide Range Supply Voltage	+6.5	-	+14.4	V
Ta	Ambient Temperature	-40	-	+85	°C
■ Thermal Information					
Rth(j-a)	Thermal resistance from junction to ambient. (Note 2)	-	12.92	-	°C/W

NOTES:
1. V_{DS} (Drain to Source) specification for internal high-side and low-side MOSFETs.
2. Rth(j-a) is measured with the component mounted on an effective thermal conductivity test board on 0 LFM condition. The test board size is 114.5mm×101.5mm×1.6mm with 4 layers. The test condition is complied with JEDECE EIJ/JESD 51 Standards.

ELECTRICAL SPECIFICATIONS: (Cont.)

Conditions: T_A = 25 ºC, unless otherwise specified.
Vin=12V, Vout=1.5V, Cin=220uF×1, 10uF/Ceramic×2, Cout=330uF/POS-CAP×1, 22uF/Ceramic×3

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
■ Input Characteristics						
$I_{Q(VIN)}$	Input supply bias current	Iout = 0A Vin = 12V, Vout = 1.5V PVCC = 12V	-	10	-	mA
$I_{S(VIN)}$	Input supply current	Iout = 10A Vin = 12V, Vout = 1.5V PVCC = 12V	-	1.48	-	A
■ Output Characteristics						
$I_{OUT(DC)}$	Output continuous current range	Vin=12V, Vout=1.5V	0	-	10	A
$\Delta V_{OUT}/\Delta V_{IN}$	Line regulation accuracy	Vin = 3.3V to 15V Vout = 1.5V, Iout = 0A Vout = 1.5V, Iout = 10A PVCC = 12V	-	0.1	-	%
$\Delta V_{OUT}/\Delta I_{OUT}$	Load regulation accuracy	Iout = 0A to 10A Vin = 12V, Vout = 1.5V PVCC = 12V	-	0.5	-	%
$V_{OUT(AC)}$	Output ripple voltage	Iout = 10A Vin = 12V, Vout = 1.5V PVCC = 12V	-	30	-	mVp-p
■ Dynamic Characteristics						
ΔV_{OUT-DP}	Voltage change for positive load step	Iout = 0A to 5A Current slew rate = 2.5A/uS Vin = 12V, Vout = 1.5V PVCC = 12V	-	75	-	mVp-p
ΔV_{OUT-DN}	Voltage change for negative load step	Iout = 5A to 0A Current slew rate = 2.5A/uS Vin = 12V, Vout = 1.5V PVCC = 12V	-	75	-	mVp-p
■ Control Characteristics						
I_{PVCC}	PVCC operating current	Iout = 10A Vin = 12V, Vout = 1.5V 5V supply 12V supply	-	 25 50	-	mA
V_{PORR}	Rising PVCC threshold	Note 3	3.9	4.1	4.3	V
V_{PORH}	PVCC Power-On-Reset threshold hysteresis	Note 3	0.30	0.35	0.40	mV

ELECTRICAL SPECIFICATIONS: (Cont.)

Conditions: T_A = 25 ºC, unless otherwise specified.
Vin=12V, Vout=1.5V, Cin=220uF×1, 10uF/Ceramic×2, Cout=330uF/POS-CAP×1, 22uF/Ceramic×3

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
■ Control Characteristics						
V_{REF}	Referance voltage	Note 3	0.591	0.6	0.609	V
F_{OSC}	Oscillator frequency	Note 3	510	600	660	kHz
R_{FB-TI}	Internal resistor between VOUT and FB pins		9.66	9.76	9.85	kΩ
V_{ENDIS}	Disable threshold voltage (COMP/EN)	Note 3	0.375	0.4	0.425	V
■ Fault Protection						
R_{SEN-IN}	Internal resistor between ISEN and PGND pins		11.97	12.1	12.22	kΩ
I_{SEN}	ISEN current source	Note 3	18.0	21.5	23.5	uA

NOTES:
3. Parameters guaranteed by PWM IC vendor design and test prior to module assembly.

TYPICAL PERFORMANCE CHARACTERISTICS: (Efficiency)

Conditions: T_A = 25 ºC, unless otherwise specified.
Cin=10uF/Ceramic×5, Cout=330uF/POS-CAP(ESR=10mΩ)×1, 22uF/Ceramic×3,
Test Board Information: 80mm×80mm×1.6mm, 4 layers, 1oz.

NOTES:

4. The efficiency measurement is $\frac{P_{OUT}}{P_{IN}+P_{PVCC}} = \frac{V_{OUT}\times I_{OUT}}{(V_{OUT}\times I_{OUT})+(V_{PVCC}\times I_{PVCC})}$

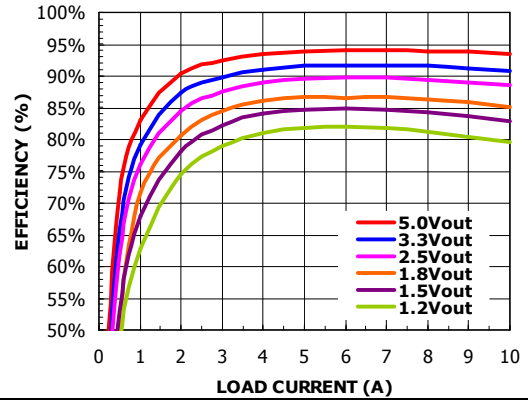


FIG.2 EFFICIENCY V.S. LOAD CURRENT (12VIN,12PVCC)

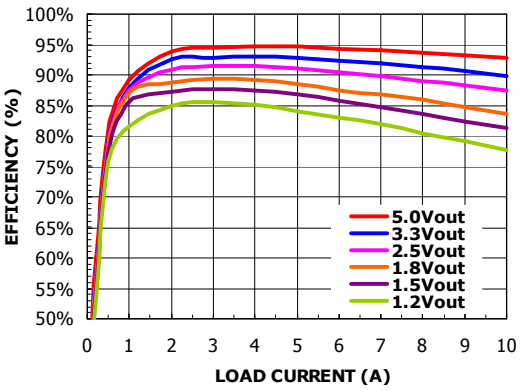


FIG.3 EFFICIENCY V.S. LOAD CURRENT (12VIN,5PVCC)

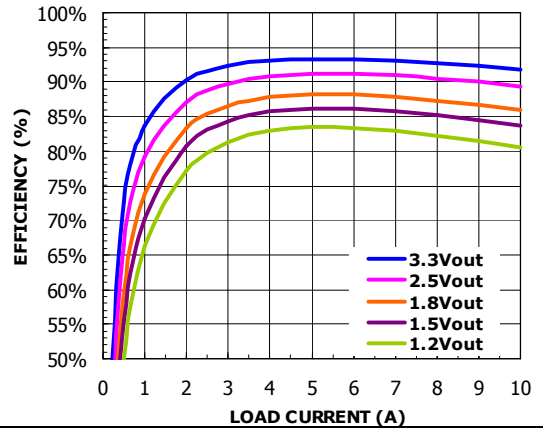


FIG.4 EFFICIENCY V.S. LOAD CURRENT (5VIN,12PVCC)

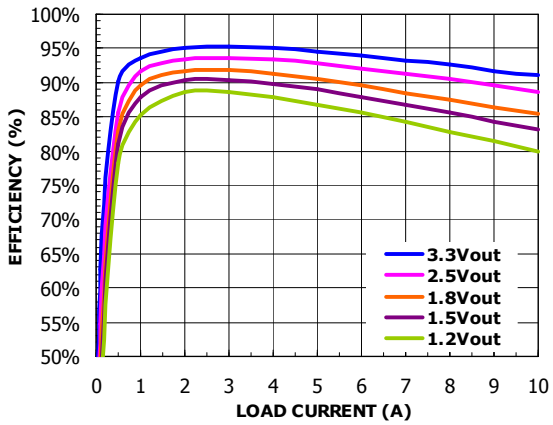


FIG.5 EFFICIENCY V.S. LOAD CURRENT (5VIN,5PVCC)

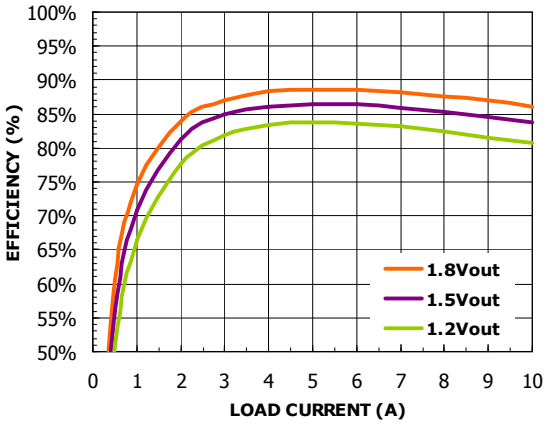


FIG.6 EFFICIENCY V.S. LOAD CURRENT (3.3VIN,12PVCC)

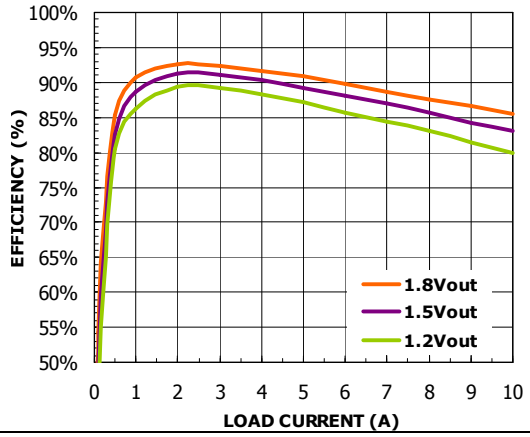


FIG.7 EFFICIENCY V.S. LOAD CURRENT (3.3VIN,5PVCC)

TYPICAL PERFORMANCE CHARACTERISTICS: (Output Ripple)

Conditions: T_A = 25 ºC, unless otherwise specified.
Vin=12V, PVCC=12V, Cin=10uF/Ceramic×5, Cout=330uF/POS-CAP(ESR=10mΩ)×1, 22uF/Ceramic×3

NOTES:

5. The output ripple measurement is short loop probing and 20MegHz bandwidth limited.

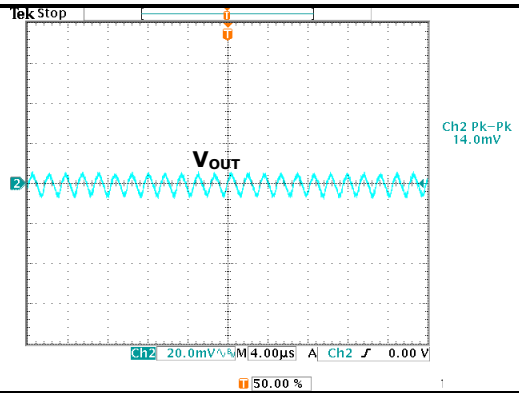


FIG.8 1.5VOUT OUTPUT RIPPLE, at 0A LOAD CURRENT

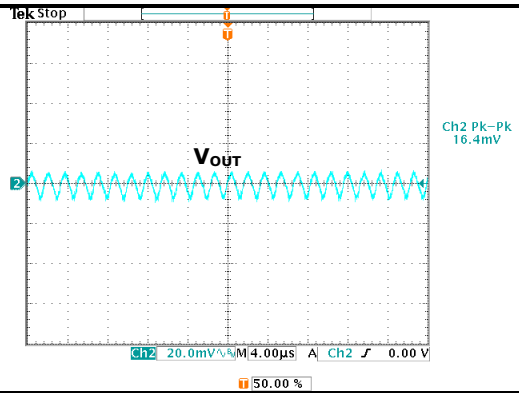


FIG.9 1.5VOUT OUTPUT RIPPLE, at 10A LOAD CURRENT

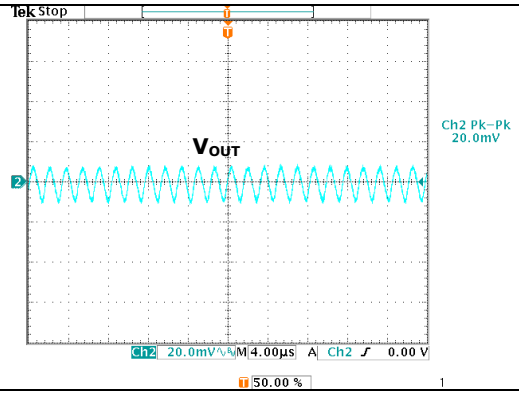


FIG.10 2.5VOUT OUTPUT RIPPLE, at 0A CURRENT LOAD

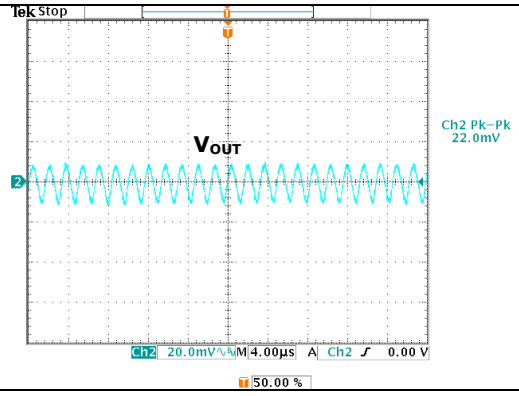


FIG.11 2.5VOUT OUTPUT RIPPLE, at 10A LOAD CURRENT

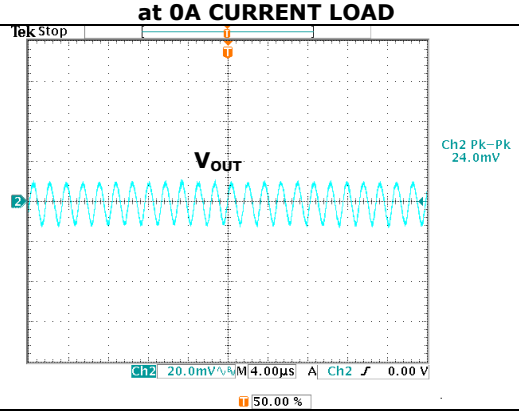


FIG.12 3.3VOUT OUTPUT RIPPLE, at 0A LOAD CURRENT

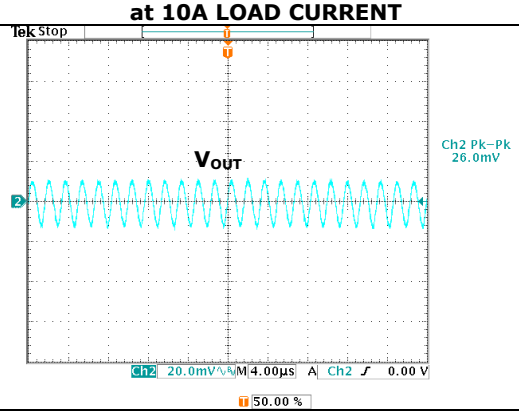


FIG.13 3.3VOUT OUTPUT RIPPLE, at 10A LOAD CURRENT

TYPICAL PERFORMANCE CHARACTERISTICS: (Transient Response)

Conditions: T_A = 25 ºC, unless otherwise specified.
Vin=12V, PVCC=12V, Cin=10uF/Ceramic×5, Cout=330uF/POS-CAP(ESR=10mΩ)×1, 22uF/Ceramic×3, Current Slew Rate=2.5A/uS

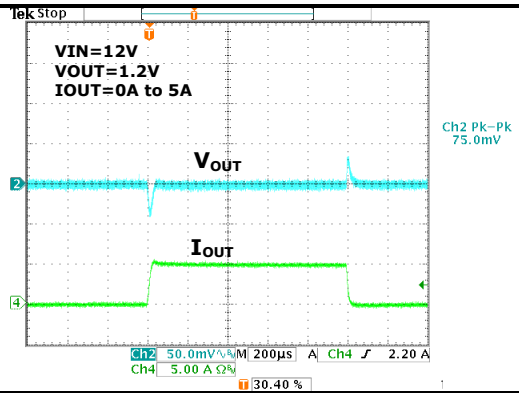


FIG.14 1.2VOUT TRANSIENT RESPONSE, at 0A to 5A LOAD CURRENT

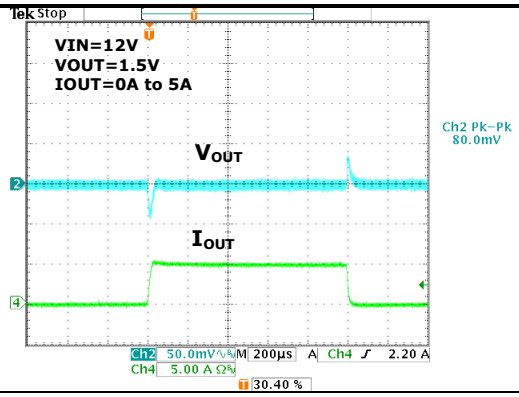


FIG.15 1.5VOUT TRANSIENT RESPONSE, at 0A to 5A LOAD CURRENT

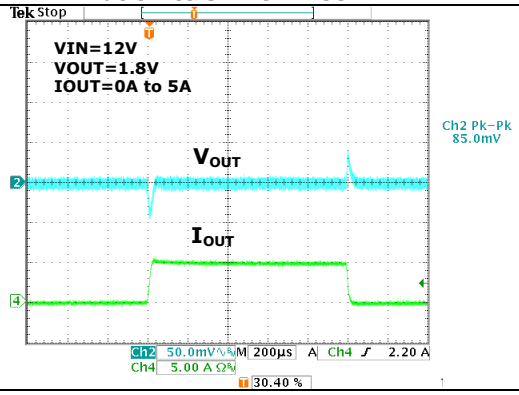


FIG.16 1.8VOUT TRANSIENT RESPONSE, at 0A to 5A LOAD CURRENT

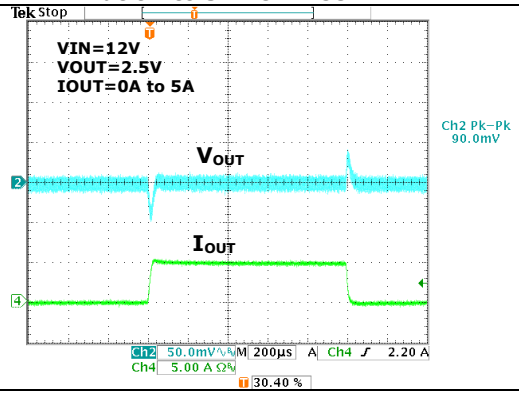


FIG.17 2.5VOUT TRANSIENT RESPONSE, at 0A to 5A LOAD CURRENT

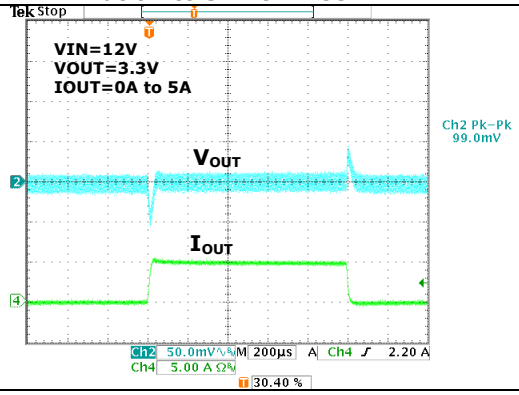


FIG.18 3.3VOUT TRANSIENT RESPONSE, at 0A to 5A LOAD CURRENT

APPLICATIONS INFORMATION:

REFERENCE CIRCUIT FOR GERNERAL APPLICATION:

The Figure 19 shows the HM10107A application schematics for input voltage +5V or +12V. The PVCC pin can connect to input supply directly.

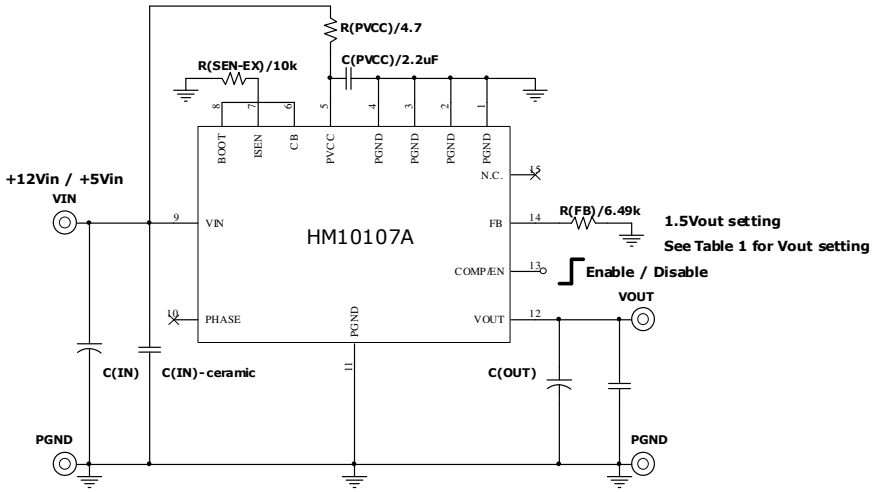


FIG.19 TYPOCAL APPLICATION WITH SINGLE POWER SUPPLY

The Figure 20 shows the HM10107A application schematics for wide input voltage from +1V to +15V. The PVCC supply can source +5V / +12V or +6.5V to +14.4V. Please refer to input voltage consideration in application information.

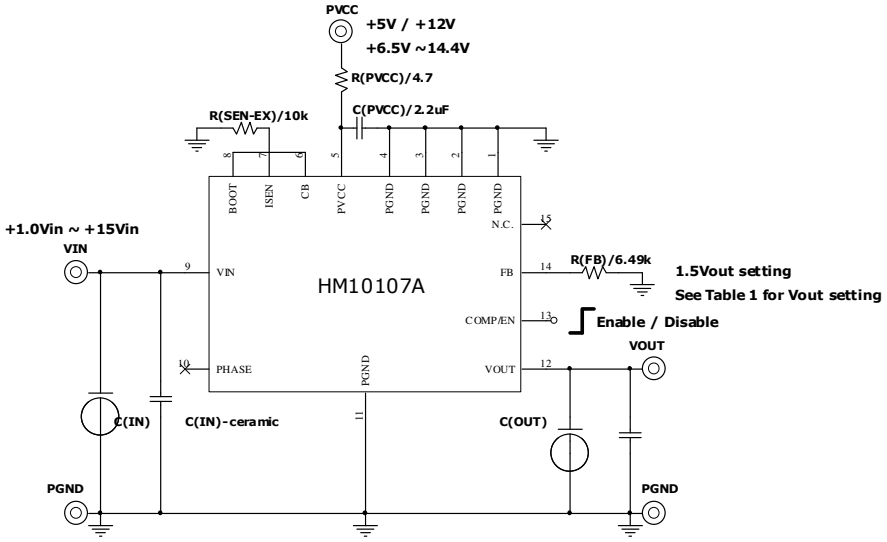


FIG.20 TYPICAL APPLICATION WITH SEPARATED POWER SUPPLY

APPLICATIONS INFORMATION: (Cont.)

PROGRAMMING OUTPUT VOLTAGE:

The HM10107A has an internal 0.6V±1.5% reference voltage. It only programs the dividing resistance R_{FB} which respects to FB pin and PGND. The output voltage can be calculated as shown in Equation 1 and the resistance according to typical output voltage is shown in TABLE 1.

$$VOUT = 0.6 \times \left(1 + \frac{9.76k}{R_{FB}}\right) \quad \text{(EQ.1)}$$

ON/OFF CONTROL:

Figure 21 shows a remote ON/OFF control of HM10107A by using COMP/EN pin. Pulling COMP/EN low than threshold voltage (V_{ENDIS}=0.4 typ.) will be disabled the HM10107A. The external pull-down device (open drain or open collector devices) will initially need to overcome maximum of 5mA of COMP/EN output current. However, once the HM10107A is disabled and still PVCC voltage bias applied, the 20uA current source will continue to draw current from COMP/EN. The turn-on waveforms with remote ON/OFF control are shown in Figure 22 and 23 for 1.5Vout applications. While the ON/OFF control was not used, leave COMP/EN pin open, the HM10107A will be following PVCC threshold voltage (V_{PORR}=4.1V typ.) to turn-on.

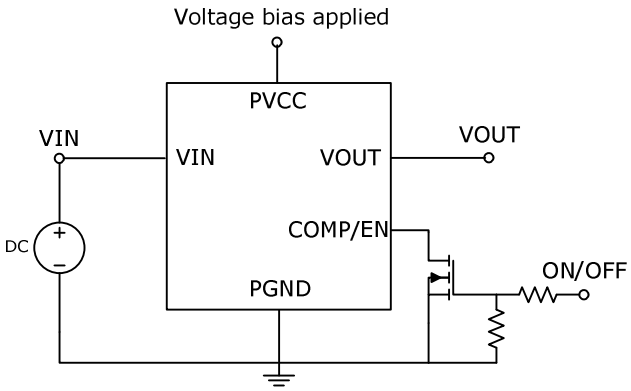


FIG.21 REMOTE ON/OFF CONFIGURATION

APPLICATIONS INFORMATION: (Cont.)

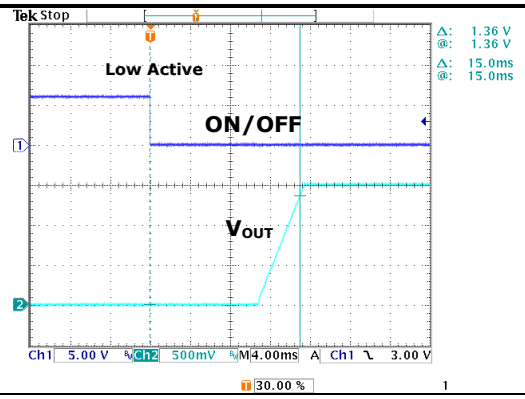


FIG.22 TURN-ON DELAY TIME at 12VIN, 12PVCC, 1.5VOUT, 10A LOAD CURRENT

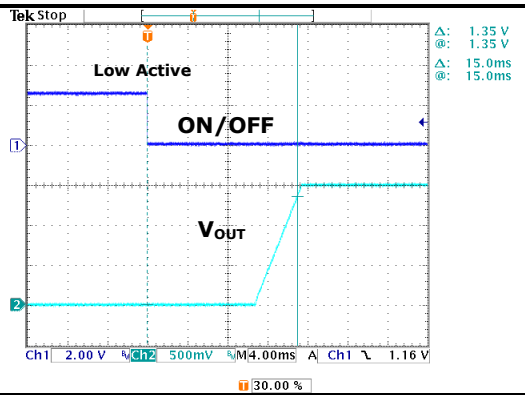


FIG.23 TURN-ON DELAY TIME at 5VIN, 5PVCC, 1.5VOUT, 10A LOAD CURRENT

SOFT-START AND PRE-BIASED OUTPUTS:

The soft-start internally ramps the reference on the non-inverting terminal of the error amp from 0V to 0.6V in a nominal 6.8mS. The output voltage will follow this ramp, from zero to final regulation value for set point. This mechanism provides output voltage soft rise and no inrush current charges the output capacitors. The entire start-up sequence from Power-on-rest typically takes up to 17mS; up to 10.2mS for delay and OCP sample and 6.8mS for the soft-start ramp.

If the output is pre-biased to a voltage less than the expected value, as shown Figure 24, the HM10107A will detect that condition. Neither internal MOSFET will turn on until the soft-start ramp voltage exceeds the output; VOUT starts seamlessly ramping from there. If the output is pre-biased to a voltage above the expected value shows as Figure 25. Neither MOSFET will turn on until the end of the soft-start, at which time it will pull the output voltage down to the final value.

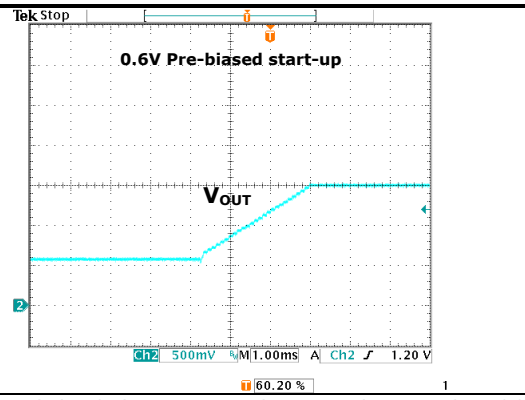


FIG.24 0.6V PRE-BIASED at 12VIN, 12PVCC, 1.5VOUT

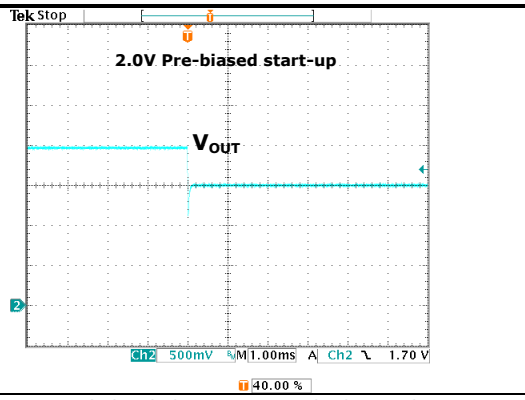


FIG.25 2.0V PRE-BIASES at 12VIN, 12PVCC, 1.5VOUT

APPLICATIONS INFORMATION: (Cont.)

OVER CURRENT PROTECTION:

The over-current function protects the converter from a shorted output by using the low side MOSFET on-resistance, $R_{DS(ON)}$, to monitor the current. A resistor (R_{SEN}) programs the over-current trip level. This method enhances the converter's efficiency and reduces cost by eliminating a current sensing resistor. If over-current is detected, the output immediately shuts off, it cycles the soft-start function in a hiccup mode (2 dummy soft-start time-outs, then up to one real one) to provide fault protection. If the shorted condition is not removed, this cycle will continue indefinitely. The over-current function will trip at a peak inductor current (I_{PEAK}) determined by Equation 2.

$$I_{PEAK} = \frac{2 \times I_{SEN} \times R_{SEN}}{R_{DS(ON)}} \quad \text{(EQ.2)}$$

Where:

$R_{DS(ON)}$ is typically 12mΩ including internal parasitic resistance. (at PVCC=V_{GS}=10V, I_{DS}=50A)

$R_{DS(ON)}$ is typically 14mΩ including internal parasitic resistance. (at PVCC=V_{GS}=5.0V, I_{DS}=30A)

I_{SEN} is the internal current source (21.5uA typ.).

R_{SEN} is equivalent resistance between ISEN and PGND pins. The HM10107A has integrated 12.1kΩ resistance (R_{SEN-IN}). Therefore, the equivalent resistance of R_{SEN} can be expressed in Equation 3.

$$R_{SEN} = \frac{R_{SEN-EX} \times R_{SEN-IN}}{R_{SEN-EX} + R_{SEN-IN}} \quad \text{(EQ.3)}$$

The relationships between the external R_{SEN-EX} values and typical over current protection trip level of HM10107A are shown as TABLE 2.

TABLE 2 RECOMMENDATION OCP TRIP FOR R_{SEN-EX} VALUES

R_{SEN-EX}	OCP Trip Level (Typ.) (Note 6) VIN=12V, PVCC=12V, VOUT=1.5V	OCP Trip Level (Typ.) (Note 6) VIN=12V, PVCC=5V, VOUT=1.5V
OPEN	CAUTION: Do not leave ISEN pin open.	CAUTION: Do not leave ISEN pin open.
10kΩ	18A	16A
8.2kΩ	16A	14A
6.8kΩ	14A	12A

NOTES:

6. The trip values are tested at T_A = 25 ºC, Cin=10uF/Ceramic×5, Cout=330uF/POS-CAP (ESR=10mΩ) ×1, 22uF/Ceramic×3. Test Board Information: 80mm×80mm×1.6mm, 4 layers, 1oz.

APPLICATIONS INFORMATION: (Cont.)

INPUT AND OUTPUT CAPACITORS:

Place the decoupled ceramic capacitors to control the high frequency voltage overshoot and bulk capacitor to supply the current needed each time module turns-on. The important parameters for bulk capacitor are voltage rating and the RMS current rating. For reliable operation, the bulk capacitor selects the voltage and current rating above maximum input voltage and highest RMS current required. The bulk output capacitors C_{OUT} is chosen with low enough effective series resistance (ESR) to meet the output voltage ripple and transient requirements. C_{OUT} can be low ESR tantalum capacitor, low ESR polymer capacitor or ceramic capacitor. The typical capacitance is 330uF and decupled ceramic output capacitors are used. Additional output filtering may be required by the system designer, if further reduction of output ripple or dynamic transient spike is required.

PVCC BIAS AND POWER-UP SEQUENCE CONSIDERATIONS:

The PVCC bias is either 5V (±10%) or 12V (±20%) and anywhere from 6.5V up to the 14.4V maximum. However, the range between 5.5V and 6.5V is not allowed for long-term reliability reasons, but transitions through it to voltages above 6.5V are acceptable. If the transition is slow (not a step change), the disturbance should be minimal. So while the recommendation doesn't have the output enabled during the transition through this region, it may be acceptable. The user should monitor the output for their application to see if there is any problem.

If PVCC powers up first and the VIN is not present by the time the initialization is done, then the soft-start will not be able to ramp the output, and the output will later follow part of the VIN ramp when it is applied. If this is not desired, then change the sequencing of the supplies, or use the COMP/EN pin to disable VOUT until both supplies are ready. Figure 26 shows a simple sequencer for this situation.

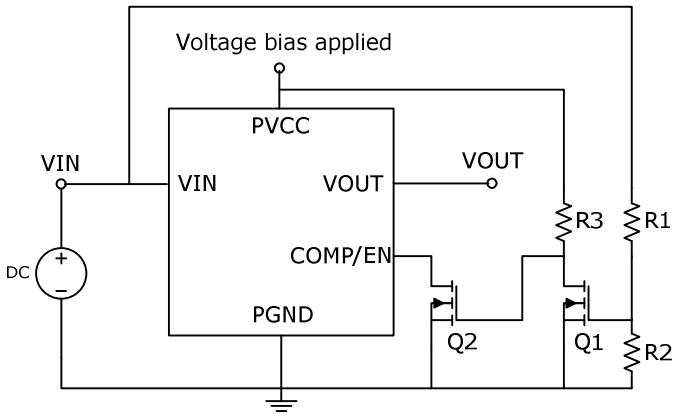


FIG.27 SEQUENCE CONFIGURATION (IF PVCC BIAS POWER-UP FIRST)

APPLICATIONS INFORMATION: (Cont.)

RECOMMENDATION LAYOUT GUIDE:

In order to achieve stable, low losses, less noise or spike, and good thermal performance some layout considerations are necessary. The recommendation layout is shown as Figure 27 and 28.

1. The ground connection between pin 11 and pin 1 to 4 should be a solid ground plane under the module. It can be connected one or more ground plane by using several Vias.
2. Place high frequency ceramic capacitors between pin 9 (VIN) and pin 11 (PGND), pin 5 (PVCC) and pin 1 to 4 (PGND) as close to module as possible to minimize high frequency noise.
3. Keep the R_{SEN-EX} and R_{FB} connection trace to the module pin 7 (ISEN) and pin 14 (FB) short.
4. Use large copper area for power path (VIN, VOUT, and PGND) to minimize the conduction loss and enhance heat transferring. Also, use multiple Vias to connect power planes in different layer.
5. Avoid layout any sensitive signal traces near the pin 10 (PHASE).

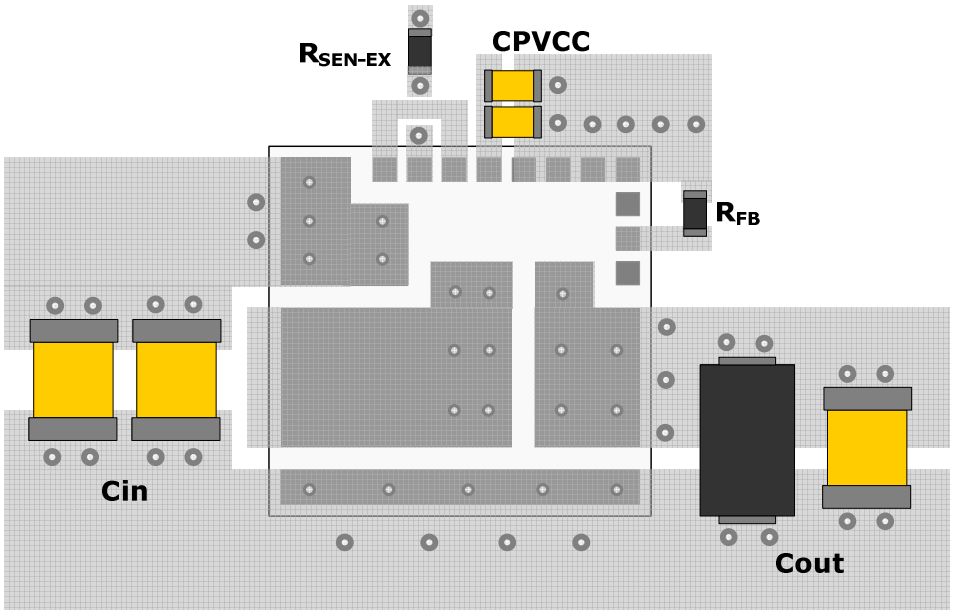


FIG.27 RECOMMENDATION LAYOUT (Top)

APPLICATIONS INFORMATION: (Cont.)

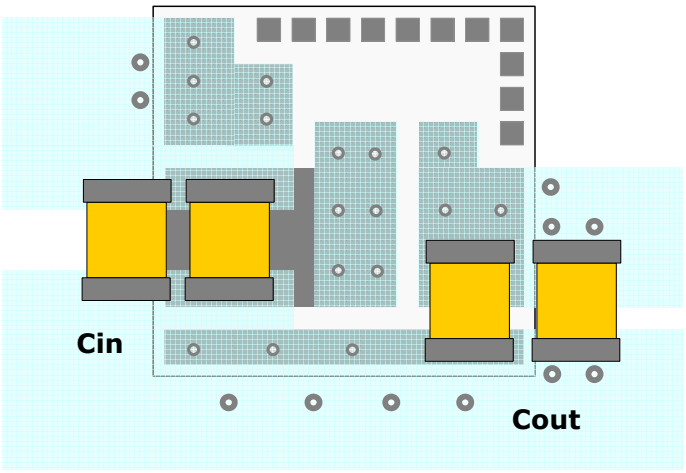


FIG.28 RECOMMENDATION LAYOUT (Bottom)

THERMAL CONSIDERATIONS:

All of thermal testing condition is complied with JEDECE EIJ/JESD 51 Standards. Therefore, the test board size is 114.5mm×101.5mm×1.6mm with 4 layers, 1oz. The case temperature of module sensing point is shown as Figure 29. Then Rth(j-a) is measured with the component mounted on a effective thermal conductivity test board on 0 LFM condition. The output current ability is function of input/ output voltage and ambient temperature factor etc. The HM10107A module is designed for using when the case temperature is below 110°C. In Figure 30 and 31, the power loss curves can be used in coordination with each load current. The load current in different input voltage are shown in Figure 32 to 35. It would be convenient for user to confirm and estimate modular's approximate performance according to actual operating conditions in beginning of design.

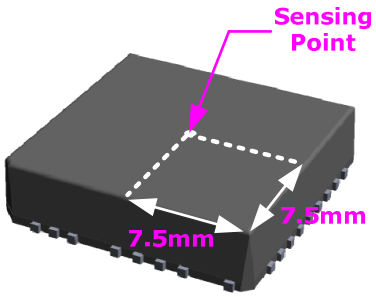


FIG.29 CASE TEMPERATURE SENSING POINT

APPLICATIONS INFORMATION: (Cont.)

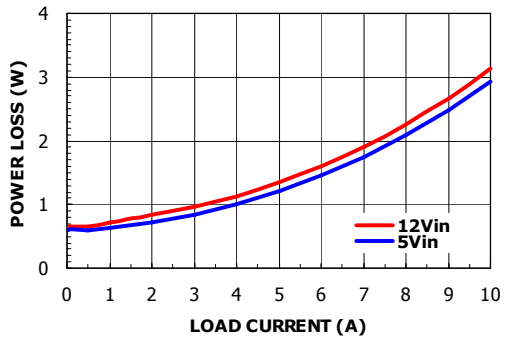


FIG.30 1.5VOUT POWER LOSS at 12PVCC

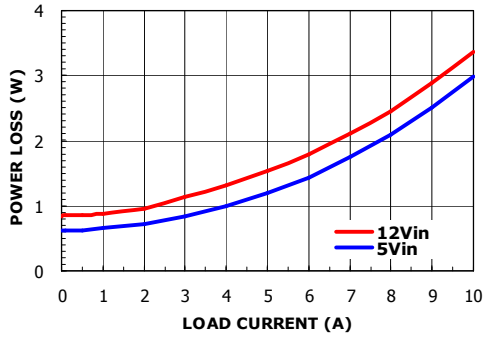


FIG.31 3.3VOUT POWER LOSS at 12PVCC

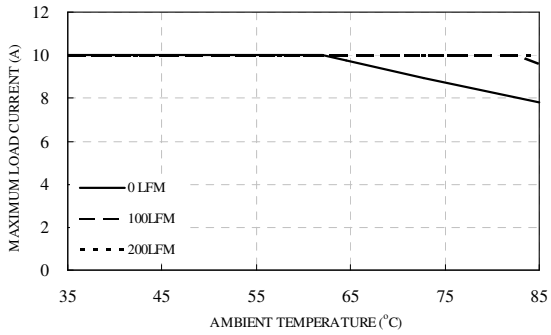


FIG.32 DE-RATING CURVE at 12VIN, 1.5VOUT, 12PVCC

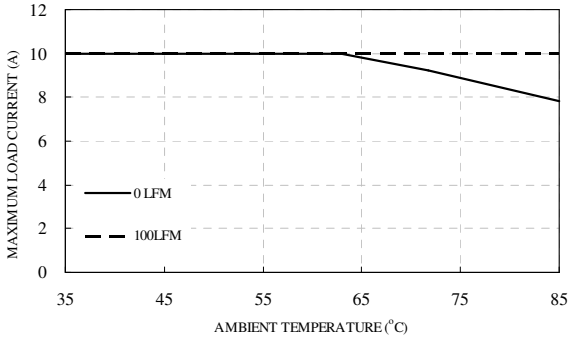


FIG.33 DE-RATING CURVE at 5VIN, 1.5VOUT, 12PVCC

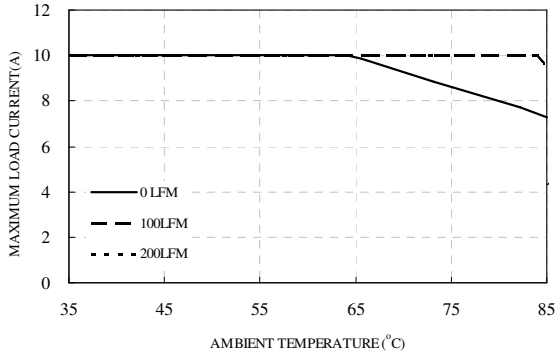


FIG.34 DE-RATING CURVE at 12VIN, 3.3VOUT, 12PVCC

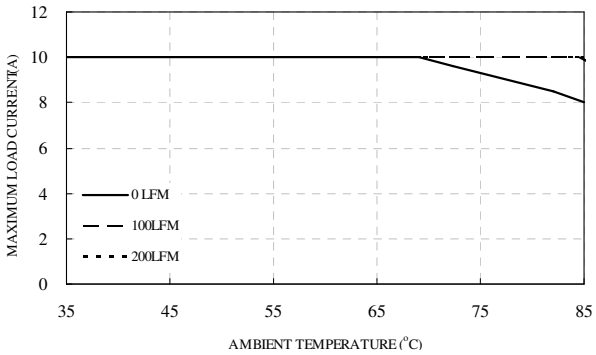
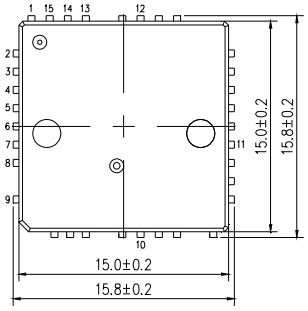


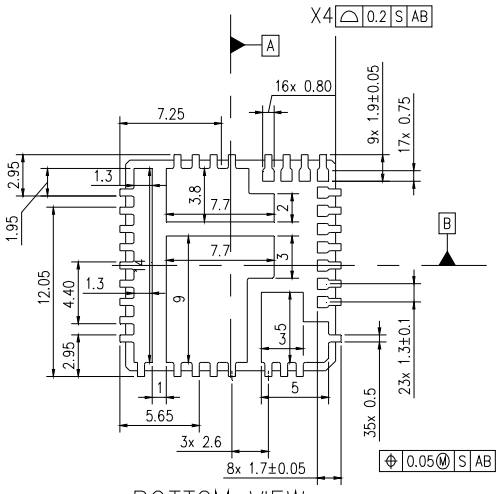
FIG.35 DE-RATING CURVE at 5VIN, 3.3VOUT, 12PVCC

PACKAGE OUTLINE DRAWING:

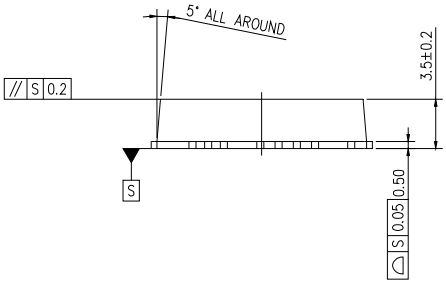
Unit: mm



TOP VIEW



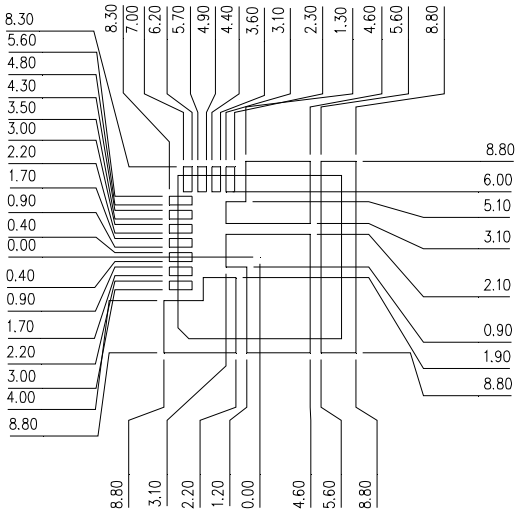
BOTTOM VIEW



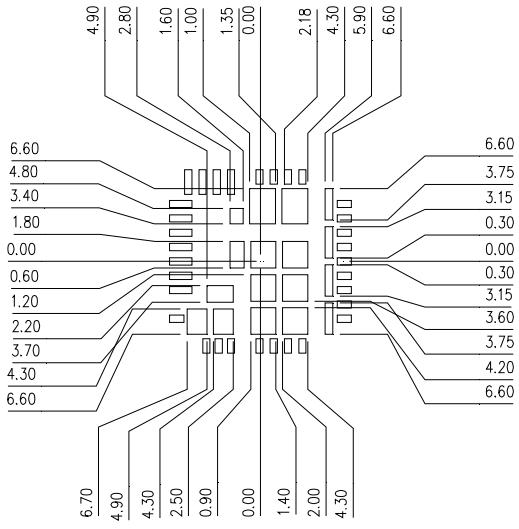
SIDE VIEW

LAND PATTERN REFERENCE:

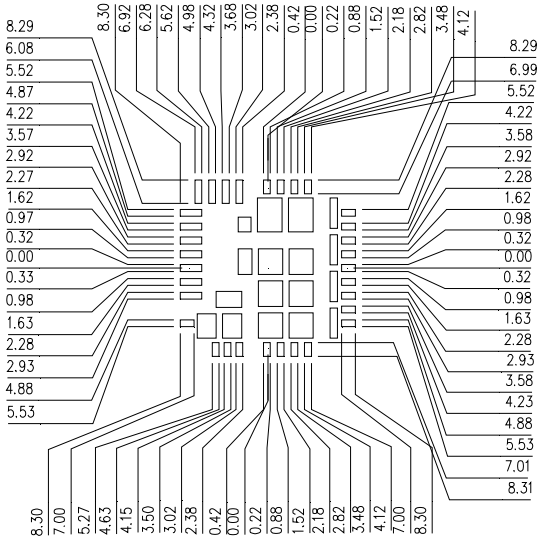
Unit: mm



TYPICAL RECOMMENDED LAND PATTERN



STENCIL PATTERN WITH SQUIRE PADS-1



STENCIL PATTERN WITH SQUIRE PADS-2

REFLOW PARAMETERS:

Lead-free soldering process is a standard of making electronic products. Many solder alloys like Sn/Ag, Sn/Ag/Cu, Sn/Ag/Bi and so on are used extensively to replace traditional Sn/Pb alloy. Here the Sn/Ag/Cu alloy (SAC) are recommended for process. In the SAC alloy series, SAC305 is a very popular solder alloy which contains 3% Ag and 0.5% Cu. It is easy to get it. Figure 36 shows an example of reflow profile diagram. Typically, the profile has three stages. During the initial stage from 70°C to 90°C, the ramp rate of temperature should be not more than 1.5°C/sec. The soak zone then occurs from 100°C to 180°C and should last for 90 to 120 seconds. Finally the temperature rises to 230°C to 245°C and cover 220°C in 30 seconds to melt the solder. It is noted that the time of peak temperature should depend on the mass of the PCB board. The reflow profile is usually supported by the solder vendor and user could switch to optimize the profile according to various solder type and various manufactures' formula.

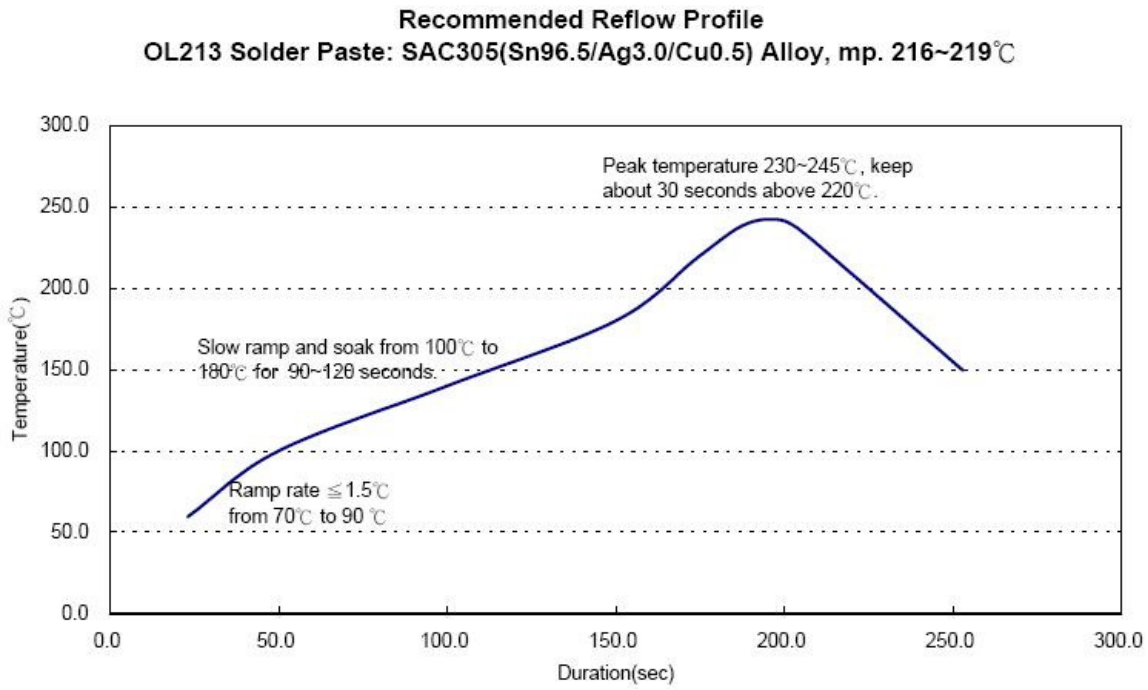


FIG.36 RECOMMENDATION REFLOW PROFILE

STORAGE AND HANDLING:

MOISTURE BARRIER BAG:

Although POL module is a kind of package devices and its inner components are all protected by the package compounds, it is still probably damaged during soldering process if moisture is absorbed into package. The modules firstly are packed in a reel, and then an aluminum moisture barrier bag is used to pack the reel in order to prevent moisture absorption. Silica gel is put into the aluminum moisture barrier bag as absorbent material.

STORAGE:

The POL module pack storage follows the JEDEC J-STD-033B01 and J-STD-020C standards. Table 3 is the floor life and moisture sensitive level defined by JEDEC. *POL module is classified into level 3.* The floor life starts to estimate while the aluminum moisture barrier bag is opened. Under the storage situation of 30°C/60% RH, the device can keep 168 hours floor life after the pack opened. If there are unused POL modules remained, they should be resealed in original moisture barrier bag as soon as possible. However, in case of the modules' floor life exceeding the defined time period, baking process will be necessary to dehumidify. The method is to bake the module in an oven at 125°C/1% RH (e.g. hot nitrogen gas atmosphere) for 48 hours.

HANDLING AND OTHERS:

To protect the POL module and to make sure its normal use, something should be noticed as below.

1. Please handle the POL module carefully to avoid unnecessary mechanism stress on it. Improperly external stress may cause unexpected damage.
2. The ESD wrist strap, ESD shoe strap or anti-electrostatic gloves are recommended to be used whenever handling POL module.
3. If cleaning the module is necessary, please use alcohol or IPA solution to clean it under normal room temperature. Avoid the use of unspecified solvent.

STORAGE AND HANDLING: (Cont.)

TABLE 3 MOISTURE CLASSIFICATION LEVEL AND FLOOR LIFE

Level	Floor Life (out of bag) at factory ambient ≦30°C/60% RH or as stated
1	Unlimited at ≦30°C/85% RH
2	1 year
2a	4 weeks
3	168 hours
4	72 hours
5	48 hours
5a	24 hours
6	Mandatory bake before use. After bake, must be reflowed within the time limit specified on the label.